CLOCK SIGNAL DISTRIBUTION UTILIZING DIFFERENTIAL SINUSOIDAL SIGNAL PAIR

Abstract of the Disclosure

A differential sinusoidal signal pair is generated on an integrated circuit (IC). The differential sinusoidal signal pair is distributed to clock receiver circuits, which may be differential amplifiers. The clock receiver circuits receive the differential sinusoidal signal pair and convert the differential sinusoidal pair to local clock signals. Power consumption and noise generation are reduced as compared to conventional clock signal distribution arrangements.

Figures